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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,193	01/14/2004	Shunpei Yamazaki	0553-0394	3577

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EXAMINER	
RAYMOND, BRITTANY L	

ART UNIT	PAPER NUMBER
1756	

DATE MAILED: 12/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/757,193	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	Brittany Raymond	1756	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-18 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-18 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 14 January 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 01142004/07252005.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1, 4, and 7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 1, 4, and 7 are indefinite because of the use of the language "forming the resist...processed under reduced pressure." It is not clear if the resist application is done under reduced pressure or if further processing is done under reduced pressure. It will be assumed that the photoresist application is done under reduced pressure, in the rejections to follow.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

4. Claims 1-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Lei (U.S. Patent Application 2004/0134420).

Lei discloses a method for bubble-free application of a resin to a substrate, wherein a photoresist layer is deposited under partial vacuum pressure onto a conductive layer, which inherently has to be formed on a substrate (Paragraph 0030),

as recited in claims 1, 4, 7, and 10 of the present invention. Lei also discloses a method of forming a pattern on a substrate, wherein the photoresist layer is exposed through a mask, the mask is then used as a pattern for etching the conductive layer, and the photoresist is then removed from the substrate (Paragraph 0033), as recited in claims 4, 7, and 10 of the present invention. Lei states that the photoresist used is a liquid photoresist (Paragraph 0029, Line 2). Therefore, it is inherent that the photosensitizer is dissolved in a solvent, as recited in claims 2, 5, 8, and 11 of the present invention. Furthermore, by definition a photoresist must contain a photosensitizer. Lei teaches that the process is used in the formation of integrated circuit patterns in the fabrication of semiconductor integrated circuits (Paragraph 0001). It is well known that semiconductor integrated circuits are used in various types of electronic devices, such as display devices, as recited in claims 3, 6, 9, and 12 of the present invention.

Thus, Lei teaches every limitation of claims 1-12 and thus anticipates the claims.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liegl (U.S. Patent Application 2004/0121264) in view of Yu (U.S. Patent Application 2005/0032378).

Liegl discloses a method of patterning an integrated circuit, comprising the steps of coating a substrate with a photosensitive layer, selectively exposing the photosensitive layer (Claim 1), and using the patterned resist as a mask for etching of the substrate (Paragraph 0016), as recited in claims 1, 4, 7, and 10 of the present invention. The substrate can include one or more device layers, which can include conductive materials (Paragraph 0009). It would have been obvious to one of ordinary skill in the art to have removed the photoresist, as recited in claims 7 and 10 of the present invention because this would be required before further processing could occur. Liegl also discloses that the photoresist comprises components, such as photosensitive compounds, which are dissolved in a solvent (Paragraph 0010), as recited in claims 2, 5, 8, and 11 of the present invention. Finally, Liegl states that the invention is used to make integrated circuits, which are used in devices such as those recited in claims 3, 6, 9, and 12 of the present invention.

Liegl fails to disclose that the substrate is coated with the photosensitive layer, which is applied under reduced pressure.

Yu discloses a method for making a precise structure which comprises the steps of depositing a layer of resist material over a wafer, selectively removing portions of the

resist layer, and etching the wafer by using the resist material as a mask (Claim 1). Yu states that the resist material is deposited onto the wafer using vacuum coating (Claim 15), or reduced pressure, as recited in claims 1, 4, 7, and 10 of the present invention.

It would have been obvious to one of ordinary skill in this art, at the time of invention by applicant, to have modified the process of Liegl, by depositing the resist material under reduced pressure, as suggested by Yu, because Yu teaches that vacuum coating is a conventional manner of coating a wafer with photoresist.

7. Claims 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lei (U.S. Patent Application 2004/0134420) in view of Park (U.S. Patent Application 2003/0202132).

The teachings of Lei have been discussed in Paragraph 4 above.

Lei fails to disclose the steps of the method recited in claims 13-15 of the present invention.

Park discloses a method of manufacturing a liquid crystal display device which include the steps of: depositing a first metal layer onto a substrate, patterning the metal layer to form a gate line with a gate electrode, placing an insulating layer over the gate electrode, depositing an amorphous silicon layer over the gate insulating layer, patterning the amorphous silicon layer to form a semiconductor island, depositing a second metal layer onto the semiconductor island, patterning the second metal layer to form a source electrode, forming a passivation film over the surface of the substrate, depositing a conductive layer on the passivation film, applying a negative photoresist onto the conductive layer, exposing the resist using a mask, patterning the conductive

layer to form a pixel electrode, and baking the material to remove unwanted resist (Claim 1), all of which are recited in claim 13 of the present invention. The steps of patterning use a step-and-repeat exposure technique, which comprises front-side exposure (Paragraph 0057) of the substrate. The patterning steps are also recited in claim 13 of the present invention. Park states that only one of each type of electrode is formed. However, it would have been obvious to one of ordinary skill in the art at the time of invention to have repeated the process to form the desired device with the desired number of conductive layers to form a functional device. Finally, Park is teaching a method for manufacturing a liquid crystal display device, which is recited in claim 15 of the present invention.

It would have been obvious to one of ordinary skill in this art, at the time of invention by applicant, to have used a photoresist in the process of patterning the source and gate electrodes, as taught by Lei, in the process of manufacturing a crystal display device of Park because Lei teaches that the photolithographic process of patterning a substrate using a photoresist is used to make circuit patterns, which could be components such as electrodes. It would have been obvious to have applied the photoresist as taught by Lei in the process of Park because this is a common process for coating a liquid photoresist on a substrate with the prevention of the formation of air bubbles in the photoresist layer which would lead to undesired imperfect pattern formation.

8. Claims 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lei (U.S. Patent Application 2004/0134420) in view of Park (U.S. Patent Application

2003/0202132) as applied to claims 1-12 above, and further in view of Hagino (U.S. Patent 5380670).

The teachings of Lei and Park have been discussed in Paragraph 7 above.

Lei and Park fail to disclose that channel protective layers are formed on the semiconductor islands and that a plurality of second semiconductor islands are formed over the channel protective layers.

Hagino discloses a method for fabricating a semiconductor device comprising forming a plurality of semiconductor islands on a top surface of a first part of a semiconductor layer (Claim 5) and forming a second plurality of semiconductor islands on the top surface of a second part of a semiconductor layer, wherein the second plurality of semiconductor islands are aligned with the first plurality of semiconductor islands (Claim 6) and a semiconductor layer being placed between the two types of islands, as recited in claim 16 of the present invention, which can be used as a protective layer.

It would have been obvious to one of ordinary skill in this art, at the time of invention by applicant, to have modified the process of manufacturing a crystal display device of Park and Lei by forming a plurality of second semiconductor islands on top of the first semiconductor islands, with protective layers in between, as suggested by Hagino because Hagino teaches that this is a common technique in the fabrication of semiconductor devices and semiconductor islands are common components formed on semiconductor devices.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brittany Raymond whose telephone number is 571-272-6545. The examiner can normally be reached on Monday through Friday, 8:00 a.m. - 4:30 p.m. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Huff can be reached on 571-272-1385. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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